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EXAMINER
ENGLUND, TERRY LEE

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,058	YONEZAWA, KATSUYUKI	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the corresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *02 December 2002* is: a)☒ approved b)☐ disapproved by the Examiner

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

The Request for Continued Examination (RCE) and Amendment submitted on Jul 31, 2003 were reviewed and considered with the following results:

The RCE was approved and entered.

The amended changes to the specification created new objections described later in the appropriate section.

Although page 11 of the amendment indicates the cancellation of claims 2, 3, 8, and 9 render their objections moot, the previous Office Action (dated Feb 24, 2003 and mailed Mar 12, 2003) cited no claim objections. Therefore, it is not understood what was being referred to.

However, the cancellation of claims 1-3, 5, and 7-9 has rendered all of their rejections (under 35 U.S.C. 112 and 35 U.S.C. 103(a)) moot.

Newly added claims 10-15 have their own respective objections and rejections, which are described later under the appropriate section.

Specification

The disclosure is objected to because of the following informalities: Page 11 of the amendment indicates the changes to the specification were made to indicate diode-connected transistors as shown in Figs. 9 and 11. However, the changes do not reflect what is actually shown. As presently amended, the descriptions of diode-connected transistors Q36-Q39 (Q56-Q59) and transistors Q40 (Q60) are now reversed. For example, Fig. 9 clearly shows transistors Q36-Q39 connected in parallel, wherein transistor Q40 is shown as being a diode-connected (i.e. common connection of its collector and base) transistor. Similarly, Fig. 11 clearly shows

transistors Q56-Q59 connected in parallel, wherein transistor Q60 is shown as being diode-connected. Appropriate corrections are required.

Claim Objections

Claims 10-15 are objected to because of the following informalities: To minimize possible confusion, it is suggested a comma be added after "circuit" and "capacitor" on lines 2 and 3, respectively in each of claims 10-13. This will more clearly indicate the "first circuit" comprises the first/second differential circuits. Since the "emitter electrode" had already been identified, it is suggested the second occurrence of "an" on line 11 of claim 10 be changed to --said--. For similar reasons, "an" on line 21 of claim 10 should also be changed to --said--. Claim 10, lines 35-36 "said second circuit, said second circuit" is redundant and should be changed to --said second circuit--. It is suggested claim 11 identify "n" after its first occurrence within the claim on line 8. For example, --(where n is an integer greater than 1)-- could be added after "stages" on line 9. Also, "2-n" should be changed to --2^{nd} to n-- on lines 12, 15, 26, and 29 of claim 11 to minimize the possibility "2-n" could be interpreted as meaning two stages minus the "n" number of stages. To help distinguish between the transistors of the first and second differential circuits within claim 11, it is suggested --first-- be added prior to "transistor" (or "transistors") on lines 9, 11, 12, and 16, and --second-- be added prior to "transistor" (or "transistors") on lines 23, 25, 26, and 30 of the same claim. These changes will also provide clear antecedent basis for "said second transistors" recited on claim 11's line 38. For consistent labeling within claim 11, it is suggested --vertical-- be added prior to "stage" on lines 14 and 28. To improve word flow, it is suggested --are-- be added prior to "connected" on line 18 of claim 11. Claim 11, lines 45-46 "said second circuit, said second circuit" is redundant and should be

changed to --said second circuit--. Since the "second terminal of said capacitor" has not been previously recited, it is suggested "the" on line 21 of claim 12 be changed to --a--. Since the emitter electrodes had been previously recited, it is suggested "an", on both lines 8 and 17 of each of claims 14 and 15, be changed to --said--. Appropriate corrections required.

Claim Rejections under 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claim 10-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. It is not clear in claim 10, lines 2-3 and 36-37, what part (e.g. terminal) of the first/second circuits is actually connected to the terminals of the capacitor. It is not understood if "a circuit input terminal and a circuit output terminal" on line 5 of claim 10 refers to the terminals of the filter circuit, first circuit, or first differential circuit. Related to this, the connections of the second differential circuit within claim 10 are misleading and/or inaccurate. Using the applicant's own Fig. 1 as an example, if 16A is considered the second differential circuit within first circuit 15A,16A, the base of second transistor Q20 is not connected to "said circuit input terminal" (assumed to be terminal 11) as recited on lines 16-17, and the four parallel transistors Q16-19 are not "diode-connected" as recited on lines 18-19. However, diode-connected transistors Q12-Q15 and second transistor Q20 do have their respective base/collector connected to a first connection node A as recited in lines 25-29. If the first circuit comprises 15A and 15B of Fig. 1, then second differential circuit 15B does have second transistor Q21, and four diode-connected parallel transistors Q22-Q25. However, the base of second transistor Q21 is not

connected to "said circuit input terminal"; 15B is connected to the second terminal of capacitor 17 even though the first circuit is supposedly connected to the first terminal of the capacitor (as recited on lines 2-3); and first connection node A is not connected to both the four diode-connected transistors Q12-Q15 of first circuit 15A and the base/collector of second transistor Q21 as recited within lines 25-29. The use of "a second circuit having an identical configuration...including a second circuit input terminal" on lines 33-35 of claim 10 is confusing. As presently written, the limitations can imply that the second circuit includes a second set of input and output terminals, since the first circuit apparently already has its own set of terminals. It is not clear in claim 11, lines 2-3 and 46-47, what part (e.g. terminal) of the first/second circuits is actually connected to the terminals of the capacitor. Claim 11, lines 9-10 and 23-24 appear to indicate the transistor and the four diode-connected transistors are connected in parallel. Therefore, it is suggested --four parallel diode-connected transistors-- replace the present "four diode-connected transistors connected in parallel with each other" on each set of lines. Similar to claim 10, the connections of the second differential circuit within claim 11 are misleading and/or inaccurate. For example, according to page 13 of the amendment, the limitations within claim 11 correspond to the applicant's Fig. 6. However, if 16A1 is considered the second differential circuit, it does not comprise the "four diode-connected transistors connected in parallel" as recited on lines 23-24. However, if 15B1 is considered the second differential circuit, it is not connected to the first terminal of capacitor 17 as implied by lines 2-3, and the base/collector of second transistor Q21 is not connected to the bases/collectors of transistors Q12 of first differential circuit 15A1 at a first connection node as recited within lines 34-38. Also related to the first connection node, lines 34-40 of claim 11 indicate the diode-

connected transistors within each of the first differential circuit's vertical stages, and the second transistors within each of the second differential circuit's vertical stages, are connected in common. However, Fig. 6 shows only the first vertical stage of both differential circuits are connected to common node 18. If the applicant's Fig. 7 is considered, although each of the respective vertical stages can are considered to have a common connection node to a current source, the vertical stages are coupled in parallel, instead of being in series as the limitations of claim 11 recite. The use of "a second circuit having an identical configuration... including a second circuit input terminal" on lines 43-45 of claim 11 is confusing. As presently written, the limitations can imply that the second circuit includes a second set of input and output terminals, since the first circuit apparently already has its own set of first terminals. Claim 12, lines 8-9 and 16-17 appear to indicate the transistor and the four diode-connected transistors are connected in parallel. Therefore, it is suggested --four parallel diode-connected transistors-- replace the present "four diode-connected transistors connected in parallel with each other" on each set of lines. The relationships between "said first terminal of said capacitor" and input/output terminals on lines 13-15 of claim 12 are not clear. For example, is the capacitor's first terminal connected to either the first circuit's input, output, or an unidentified terminal? As presently recited, the fundamental circuits of claim 12 are coupled between three positions (i.e. input terminal, output terminal, and the capacitor's first terminal). Clarification is requested with respect to if the second circuit of claim 12 includes an additional (i.e. second) set of input/output terminals if the circuit has "an identical configuration as said first circuit", which already has a first set of input/output terminals. The limitations recited within claim 13 should correspond to the applicant's Fig. 8. However, the plurality of fundamental circuits of the first differential circuit

are not "connected in parallel" as recited on line 5. The fundamental circuits within first differential circuit 15A3 are clearly shown being connected in series between VIN+ and VO+. Therefore, does claim 13 relate to another figure, or is the limitation inaccurate? Similar to claim 12 problems previously described, lines 8-9 and 16-17 of claim 13 appear to indicate the transistor and four diode-connected transistors can all be connected in parallel with each other; how the capacitor's first terminal relates to the first circuit's input/output terminals is not clear on lines 13-15; and lines 18-21 appear to indicate that the second circuit can also include a second set of input/output terminals. Similar to other previously described claims, the second differential circuit within claim 14 has confusing connections because they do not clearly reflect what is shown within the applicant's own figures. For example, the limitations recited within claim 14 are intended to correspond to the applicant's own Fig. 9. However, if 36A is deemed the second differential circuit, transistors Q36-Q39 are not four diode-connected transistors as recited on lines 14-15. If 35B is deemed the second differential circuit, the collector/base of second transistor Q41 is not connected in common at first connection node A with the bases/collectors of Q32-Q35 of the first differential circuit as recited within lines 25-31. Also, claim 14 appears to indicate the second circuit can have a second set of input/output terminals since the circuit has an identical configuration as the first circuit, which already has its own terminals. Claim 15 should correspond to Fig. 11, as the amendment's page 17 implies. However, the claim's limitations do not accurately correspond to what is actually shown. For example, if 56A is deemed the second differential circuit, transistors Q56-Q59 are not diode-connected as recited within lines 14-15. However, if 55B is deemed the second differential circuit, the base/collector of second transistor Q61 is not connected to the first connection node

A and bases/collectors of Q52-Q55 of first differential circuit 55A as recited within lines 25-29. Also, the figure does not show a "direct-current power supply" as recited within lines 23-24. If this supply relates to DC power supply 40 of Fig. 9, that figure does not show it being connected to any diode-connected transistor. Therefore, it is not clear if the recited limitations are accurate. Also, the "identical configuration" relationships (e.g. see lines 34-37) between the input/output terminals of the first and second circuits need to be clarified better.

Claim 10 recites the limitation "said first circuit output terminal" in lines 30-31. There is insufficient antecedent basis for this limitation in the claim. For example, does this refer to "a circuit output terminal" recited on line 4?

It is suggested that when the applicant indicates a claim corresponds to a specific figure, the claimed limitations should accurately read on the circuit structure/connections shown within that figure.

Claim Rejections under 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

In so far as being understood, claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mihailovits et al. (Mihailovits), in view of the teachings of Okanobu. [Both of these references were cited in the previous Office Action.] Fig. 2 of Mihailovits shows a filter circuit comprising three stages 260-280, wherein each stage comprises a pair of differential circuits. The stages are coupled in series between input/output terminals. For example,

differential circuits 201,202 and 203,204 of stage 260 receive input signal Vin at input terminals 150,160, and provide outputs to the input terminals (i.e. bases of 205,208) of stage 270. The bases of b05,208 correspond to the output terminals of stage 260. One of ordinary skill in the art would understand stages 260, 270, and 280 are coupled in series between the input terminals (receiving Vin) and output terminals (providing Vout). Also, these series coupled stages/ differential circuits are coupled between first and second power supplies (unlabelled but understood to represent a positive power supply and ground). Although Fig. 2 does not show the first and second differential circuits as recited within independent claim 10, each differential circuit (e.g. 201,202) of Fig. 2 can be replaced by the doublet circuit shown in Mihailovits' Fig.5 (see column 3, lines 49-51). The circuit in Fig. 5 shows a first differential circuit comprising one transistor 501 and diode-connected transistor 503 (with an emitter area n-times the area of 501) with their emitter electrodes connected together to a second power supply (e.g. ground) through first current source 505. Also shown in Fig. 5 is a second differential circuit comprising one diode-connected transistor 504 and transistor 502 (with an emitter area n-times the area of 504) with their emitter electrodes connected together to the second power supply through second current source 506. The upper current source IBIAS is coupled to a common connection point of diode-connected transistors 503 and 504. However, the reference of Mihailovits does not show or disclose diode-connected transistor 503 and transistor 502 of Fig. 5 as four parallel connected diode-connected transistors and transistors, respectively. Okanobu shows/discloses three examples of functionally equivalent differential circuits in Figs. 2, 5, and 6. Of special interest, with respect to the present application, differential circuit Q1,Q2 of Okanobu's Fig. 2 (having a ratio of 1:N) corresponds to differential circuit Q1,Q21-Q24 of Okanobu's Fig. 5, wherein the

single transistor Q2 (with an emitter area of N) of Fig.2 has been replaced by four (a plurality of) parallel-connected transistors Q21-Q24. From the knowledge of one of ordinary skill in the art, and from what Okanobu discloses (e.g. see column 5, line 58 - column 6, line 19), it would have been obvious to one of ordinary skill in the art to replace Mihailovits' diode-connected transistor 503 with an n-number of parallel diode-connected transistors (each having an area A), and also replace transistor 502 with an n-number of parallel connected transistors (each having an area A). Since Mihailovits discloses the emitter area ratio is typically between 4 and 5 (see column 3 , lines 46-48), it would be understood the ratio typically ranges between 4:1 and 5:1. Therefore, it also would have been obvious to one of ordinary skill in the art to let N = 4, and replace diode-connected transistor 503 with four parallel diode-connected transistors, and also replace transistor 502 with four parallel connected transistors. With such a modification, Mihailovits' Fig. 5 corresponds to the applicant's own Fig. 1 first/second differential circuits 15A/16A. More specifically, Mihailovits' transistors 501,502; diode-connected transistors 503,504, upper current source IBIAS, input Vin, and current sources 505/506 correspond to the applicant's Fig. 1 transistors Q11,Ql 6-Q1 9, diode-connected transistors Q12-Q15,Q20, current source 23A, input VIN+, and current sources 21A/22A, respectively. Referring back to Mihailovits' Fig. 2, with each differential pair shown in Fig. 2 replaced by the modified Fig. 5 circuit, Fig. 5's output Vout (with respect to the replaced differential pair 201,202) would be coupled to the first (left) terminal of first capacitor 240, and with respect to the replaced differential pair 203,204, it would be coupled to the second (right) terminal of first capacitor 240. This configuration corresponds to the applicant's Fig. 1 wherein first/second differential circuits 15A/16A, capacitor 17, and first/second differential circuits 15B/16B correspond to Mihailovits' circuit 201,202, capacitor

240, and circuit 203,204, respectively, wherein each of Mihailovits' circuits is replaced by the modified Fig. 5 circuit as previously described. Using some of the reference designators shown in Fig. 2 to provide a simple example, one of ordinary skill in the art would know circuit 201-204 receives the initial input signal Vin on input terminals150,160 and provides an output to circuit 205-208, which in turn provides an output to circuit 209-212 that provides final output signal Vout. Therefore, it would be obvious to one of ordinary skill in the art that the plurality of corresponding first/second differential circuits are connected in series between the input/output terminals Vin/Vout of Fig. 2. Since modified circuit 260 of Mihailovits corresponds to the applicant's own Fig. 1, which in turn corresponds to claim 10, claim 10 is rendered obvious.

No claim is allowable as presently written.

Allowable Subject Matter

However, claims 11-15 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure a filter circuit comprises all of the limitations believed to be intended within the claims (e.g. if the claimed limitations accurately correspond to the circuitry actually shown within the applicant's own figures). For example, claims 11-15 supposedly correspond to the applicant's Figs. 6-9, and 11, respectively. Although the presently claimed limitations do not correspond to the applicant's circuits, if the claims are amended to accurately relate to those figures, there is no strong motivation to ensure each filter circuit comprises a first circuit (with first/second differential circuits), a second circuit with an identical configuration of the first circuit, and at least one connection node as recited within the claims. More specifically, 1) claim 11 requires that each

differential circuit has n vertical stages with each stage formed by the transistor(s)/diode-connected transistor(s); 2) each differential circuit comprises a plurality of fundamental circuits each formed by the transistor(s)/diode-connected transistor(s), wherein the first and second differential circuits are connected in parallel with each other as recited within claims 12 and 13; 3) besides a first connection node and first capacitor, claim 14 also requires a second connection node, second capacitor, and a direct current power supply connected to the first and second circuits; and 4) similar to claim 14, claim 15 also requires a second connection node and second capacitor.

Claims 1-9 have been cancelled.

Response to Arguments/Comments

Page 12 of the amendment indicates new independent claim 10 corresponds to the applicant's own Fig. 2. However, this is obviously an oversight since Fig. 2 shows a circuit equivalent to the circuit shown within Fig. 1. Therefore, it is understood that the limitations within claim 10 correspond to Fig. 1.

The applicant's arguments with respect to the references of Mihailovits et al. and Okanobu have been considered, but are moot in view of the new ground(s) of rejection. All of the previous claims have all been cancelled, and new claims are now recited.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (703) 308-4817. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for TC 2800 is

(703) 872-9318 for communications before a final action has been mailed, and (703) 872-9319 for communications after a final action.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

TLE
Terry L. Englund

5 September 2003

TIMOTHY P. CALLAHAN
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